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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
CRAIG, DWIN M	
ART UNIT	**PAPER NUMBER**
2123	

DATE MAILED: 09/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/777,543	FURUSAWA, SHINYA	
	Examiner	Art Unit	
	Dwin M Craig	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-9,11-13,15-19,21 and 25-29* is/are rejected.

7)☒ Claim(s) *4, 10, 14 20 and 30* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 1/26/05 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/20/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-30 have been presented for reconsideration based on Applicant's Amended claim language and arguments.

2. Regarding the Applicant providing a copy of the PTO FORM 1449, the Examiner thanks the Applicant for providing another copy of an Information Disclosure Statement. The Examiner will review the references provided in the newly submitted PTO FORM 1449.

Drawings

3. The Examiner thanks the Applicant for providing substitute drawings.

Response to Arguments

4. Applicant's arguments provided in the 6-20-2005 responses have been fully considered. The Examiner's response is as follows.

4.1 Regarding the Applicant's response to the Examiner's "Notice of Non-Compliant Amendment" the Examiner notes that that Applicant has provided a statement that the Substitute Specification introduced no new matter. The Examiner thanks the Applicant for providing the statement and withdraws the objection to the previously filed Substitute Specification.

4.2 Regarding the Applicant's response to the Examiner's rejections of claims 1-30 under 35 USC § 112 written description requirements. The Examiner thanks the Applicant for submitting a Substitute Specification and withdraws the rejections of claims 1-30 under 35 USC § 112 written description requirements.

4.3 Regarding the Applicant's response to the 35 USC § 112 first paragraph rejection based on reference numerals in the specification that refer to the Japanese Laid-Open Patent Application. The Examiner has found Applicant's arguments presented on page 17 of the 1-26-2005 responses to be persuasive and withdraws the 35 USC § 112 first paragraph rejection based on reference numerals in the drawings.

4.4 Regarding the Applicant's response to the rejection of claims 2, 12 and 22 under 35 USC §112 Second Paragraph. The Examiner thanks the Applicant for amending the claims language and the Examiner withdraws the 35 USC § 112 Second Paragraph rejections of claims 2, 12 and 22.

4.5 Regarding the Applicant's response to the rejections of claims 3, 5-9, 13, 15-19, 23 and 25-29 under 35 USC § 112 Second Paragraph, the Examiner thanks the Applicant for amending the language in claims 3, 5-9, 13, 15-19, 23 and 25-29 and withdraws the 35 USC § 112 Second Paragraph rejections of those claims.

4.6 As regards Applicant's response to the Examiner's 35 USC § 112 Second Paragraph rejection of claims 4, 14 and 24. Applicant's persuasive arguments on pages 19 and 20 of the 1-26-2005 responses have convinced the Examiner to withdraw the 35 USC § 112 Second Paragraph rejections of claims 4, 14 and 24.

4.7 As regards Applicant's responses to the Examiner's rejections of claims 1, 2, 3, 5-9, 11-13, 15-19, 21, 23 and 25-29 under 35 USC § 102(e) in view of US Patent 6,026,219.

On page 20 of the 1-26-2005 responses Applicant argued, *[For example, according to an aspect of Applicant's claimed invention, the source program for hardware description written in a programming language might be written in a programming language such as C programming language, and then compiled using a software compiler.]* The Examiner respectfully traverses Applicant's arguments. The Examiner notes the following; Applicant is arguing that a *"software compiler"* can only compiler code generated in a high level programming language, in this case the C programming language. The Examiner notes that Applicant is arguing a specific definition of a *"software compiler"*. The Examiner respectfully point out that Applicant's current claim language reads on the use of a *"software compiler"* for compiling code written in a Hardware Description Language. Applicant's are attempting to read meaning into the claim language that narrows the meaning of a *"software compiler"* that is considerably broader than the current expressly claimed limitations. The Examiner has found this argument to be unpersuasive and upholds the earlier 35 USC § 102(e) rejections of claims 1, 2, 3, 5-9, 11-13, 15-19, 21, 23 and 25-29.

4.8 Regarding the Applicant's response to the 35 USC 102(b) rejections of claims 1, 2, 3, 5-9, 11-13, 15-19, 21, 23, and 25-29 as being anticipated by US Patent 5,937,190.

Applicant's argued on page 21 of the 1-26-2005 responses, [Gregory discloses analyzing and debugging digital circuits constructed from hardware description language source text using logical synthesis or behavioral synthesis (Gregory, col. 1 lines 15-19), that the product of the logical synthesis can be refined by presentation thereof to the designer (Fig. 1, Gregory Co. 7

lines 19-25). Gregory does not disclose or suggest a source program for hardware description in a programming language that is compiled using a software compiler.] The Examiner respectfully traverses Applicant's arguments. Hardware description languages are programming languages and HDL code is compiled using a software compiler, *see Gregory Col. 13 lines 58-67.*

4.9 The Examiner has found Applicant's arguments in regards to the 35 USC § 102 rejections of the claims to be unpersuasive and upholds the prior art rejections of the claims.

Claim Interpretation

5. The Claims have been given the broadest interpretation by the Examiner. For the purposes of examination the Examiner has determined that the Applicant's claims are directed towards the verification of an electronic circuit design. Further, the Examiner notes that the claims are directed towards a comparison between a behavioral synthesis of the design being compared to a "*compiled*" version of the design, which has been programmed with a standard higher level programming language, and determining if the *behavioral* version of the design operates in the same manner as the *compiled* version of the design.

The Examiner asserts that when the Applicant is claiming, *"A hardware description verifying system"* that this system is functionally equivalent to *"a hardware description language based circuit design verification system."*

The Examiner asserts that when the Applicant is claiming, *"a storage unit which stores a source program for hardware description in a program language"* that this system is

functionally equivalent to *"a storage unit where source code for a hardware description programming language is recorded."*

The Examiner asserts that when the Applicant is claiming, *"which detects a portion of source code program different in logic interpretation between a case of compiling said source program using a compiler and a case of behavioral synthesis"* that this method is functionally equivalent to *"determining if the timing behavior of a circuit modeled using behavioral synthesis is the same as the timing verification of the same circuit which has been modeled using a design compiler."*

The Examiner asserts that when the Applicant is claiming, *"source program"* that this is functionally equivalent to *"source code"*.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the

reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

6. Independent **Claims 1, 11 and 21** and dependent **Claims 2, 3, 5-9, 12, 13, 15-19, 23 and 25-29** are rejected under 35 U.S.C. 102(e) as being clearly anticipated by **Miller et al. U.S. Patent 6,026,219.**

6.1 As regards independent **Claims 1, 11 and 21** the *Miller et al.* reference teaches a hardware description language based circuit design verification system **(Figure 2 Item 1340, *Timing Verifier*, Col. 8 Lines 47-60, Col. 25 Lines 20-31),** a storage unit where source code for a hardware description programming language is recorded **(Figure 1 Item 107, Col. 5 Lines 16-18, Col. 6 Lines 51-56, Col. 8 Lines 17-22),** an output unit **(Figure 1, Item 121 or Item 124 or Item 126 or Item 127, Col. 5 Lines 20-26, Col. 5 Lines 52-64),** a processor **(Figure 1 Item 109, Col. 4 Lines 64-67, Col. 5 Lines 1-15),** which detects a portion of source code program different in logic interpretation, *in this case timing verification* **(Figure 2 Item 1340 Timing Verification Col. 8 Lines 47-57)** between a case of compiling said source program using a compiler **(Figure 2 Item 1330, Logic Synthesis Col. 9 Lines 1-2)** and a case of behavioral synthesis **(Figure 2 Item 1300, Behavioral Synthesis Col. 8 Lines 61-67),** and outputs the existence of said source program portion to said output **(Figure 4, Col. 10 Lines 28-33** *The Examiner notes that in the specification is disclosed, "Such HDL source code is the input to the synthesis process shown." And "Such a mapped circuit is the output of step 1520."*).

6.2 As regards dependent **Claims 2, 12 and 23** the *Miller et al.* reference teaches detecting, *verifying, "clock timing"* of a *"register"* type **(Figure 17, Col. 21 Lines 51-61 Col. 22 Lines 1-8).**

6.3 As regards dependent **3, 5-9, 13, 15-19, 23 and 25-29** the *Miller et al.* reference discloses a signal list **(Figure 4 *input[1:0] a,b,c,x,y;*).**

6.4 As regards dependent **Claims 10, 20 and 30** the *Miller et al.* reference teaches an right operand of the operator type includes a variable with substitution **(Figure 4, *r <= a + b – c;*).**

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Independent **Claims 1, 11 and 21** and dependent **Claims 2, 3, 5-9, 12, 13, 15-19, 23 and 25-29** are rejected under 35 U.S.C. 102(b) as being clearly anticipated by **Gregory et al. U.S. Patent 5,937,190.**

7.1 As regards independent **Claims 1, 11 and 21** the *Gregory et al.* reference teaches a hardware description language based circuit design verification system **(Figure 1, Col. 5 Lines 15-37),** a storage unit where source code for a hardware description programming language is recorded **(Figure 2 Item 900, Col. 14 Line 62),** an output unit **(Figure 2 Item 904, Col. 7 Lines 19-25, Figure 8 Item 3840),** which detects a portion of source code program different in logic interpretation, **(Figure 1 Item 131 & 120, *Simulate function vs. Synthesize with probes* Figure**

7, Figure 8, Col. 52 Lines 35-48) between a case of compiling said source program using a compiler **(Col. 17 Lines 12-31, *note the discussion of using compilers*)** and a case of behavioral synthesis **(Col. 1 Lines 15-19),** and outputs the existence of said source program portion to said output **(Col. 24 Lines 57-60, Figure 41 Items 5520, 5570 & 5560).**

7.2 As regards dependent **Claims 2, 12 and 23** the *Gregory et al.* reference teaches substitution of a variable of a register type **(Figure 57 Item 5910, Figure 59 Figure 60 Item 6102).**

7.3 As regards dependent **3, 5-9, 13, 15-19, 23 and 25-29** the *Gregory et al.* reference discloses a signal list **(Figure 32 *"signal new_level: bit_vector(1 downto 0);"*).**

7.4 As regards dependent **Claims 10, 20 and 30** the *Gregory et al.* reference teaches a right operand of the operator type includes a variable with substitution **(Figure 18, *Z<= not (A or B)* and Figure 48 Editor 2 listing lines 324-327).**

Allowable Subject Matter

8. Claims 4, 10, 14, 20 and 30 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The following is an Examiner's Reasons for Allowance.

As regards dependent claims 4 and 14, the following limitations, in combination with other limitations are neither anticipated nor made obvious by the prior art, *"said processor*

detects said source program portion in which substitution to a variable of a non-overwrite type is carried out twice or more at a clock timing event".

As regards dependent claims 10, 20 and 30 the following limitations, in combination with other limitations are neither anticipated nor made obvious by the prior art, *"wherein the processor detects said source program portion in which a logical operator is used and a right operand of the operator type includes a variable with substitution".*

Conclusion

9. Claims 1-3, 5-9, 11-13, 15-19, 21 and 25-29 are rejected. Claims 4, 10, 14, 20 and 30 are objected to.

9.1 THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

9.2 Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dwin M. Craig whose telephone number is (571) 272-3710. The examiner can normally be reached on 10:00 - 6:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo P. Picard can be reached on (571) 272-3749. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DMC

Paul L. Rodriguez 9/19/05

Primary Examiner
Art Unit 2125